CLAIMS

What is Claimed is:

1(Previously Presented) A high speed serial memory interface system comprising:

an information configuration core for coordinating proper alignment of information communication signals;

a system interface for communicating with a system controller at a first communication rate, said system interface coupled to said information configuration core; and

a memory array interface for communicating with a memory array at a second communication rate, said memory array interface coupled to said information core, wherein said memory array is included on a same substrate as said high speed serial memory interface system.

2(Original) A high speed serial memory interface system of claim 1 wherein said system interface comprises:

a serial read data port for communicating serial read information from said system controller, said serial read data port communicates said serial read information in accordance with a first synchronized clock signal;

a serial write data port for communicating serial write information from said system controller, said serial write data port communicates said serial write information in accordance with said first synchronized clock signal; and

a serial address data port for communicating serial address information from said system controller, said serial address data port communicates said serial address information in accordance with said first synchronized clock signal.

3(Original) A high speed serial memory interface system of claim 1 wherein said memory array interface comprises:

a parallel transmit port for transmitting information to said memory array, said parallel transmit port transmits said information in accordance with a second synchronized clock signal;

a parallel receive port for receiving information from said memory array, said parallel receive port receives said information in accordance with a second synchronized clock signal;

a parallel address port for communicating address information to an address array, said parallel address port communicates said address information in accordance with a second synchronized clock signal; and

a control port for communicating control information to said memory array, said control port communicates said control information in accordance with a second synchronized clock signal.

4(Cancelled).

5(Cancelled).

6(Original) A high speed serial memory interface system of claim 1 wherein said memory array interface operates at a second clock speed that is slower than a first clock speed of operations at said system interface.

7(Original) A high speed serial memory interface system of claim 1 wherein said memory array interface deals with the reading and writing of data to and from a memory array with the address and control buses.

8(Original) A high speed serial memory interface system of claim 7 wherein said communications are synchronous to a system clock at double rated clocking.

9(Original) A high speed serial memory interface system of claim 7 wherein said serial memory interface operates at a first clock speed that is faster than a second clock speed of operations at said memory array interface

10(Previously Presented) A high speed serial memory interface system of claim 1 wherein said information configuration core includes 8B/10B encoding.

11(Previously Presented) A single chip memory module integrated high speed serial interface system comprising:

a memory module array for storing information; and

high speed serial memory interface system for providing interface configuration management of information communications between a high speed serial system controller and said memory module array, wherein said memory module array and said high speed serial memory interface system are included on a single substrate,

wherein said high speed serial memory interface system includes:

an information configuration core for coordinating proper alignment of information communication signals,

a system interface for communicating with a system controller at a first communication rate, said system interface coupled to said information configuration core

a memory array interface for communicating with a memory array at a second communication rate, said memory array interface coupled to said information core.

12(Previously Presented) A single chip memory module integrated high speed serial interface system of Claim 11 wherein said memory module array is coupled by lines internal in a single substrate to said high speed serial memory interface system without drivers.

13(Original) A single chip memory module integrated high speed serial interface system of Claim 11 wherein the single substrate is a well controlled environment and capacitive flux in the point to point connections is manageable and does not adversely impact the integrity of the communications.

14(Original) A single chip memory module integrated high speed serial interface system of Claim 11 wherein signals have low voltage swings that produce very low noise potential on each line resulting in very low noise in the system.

15(Original) A single chip memory module integrated high speed serial interface system of Claim 11 wherein data and address bits are provided synchronously upon a clock signal edge.

16(Original) A single chip memory module integrated high speed serial interface system of Claim 11 wherein said memory array interface deals with the reading and writing of data to and from a memory array with the address and control buses.

17(Previously Presented) A high speed serial memory interface method comprising:

engaging in serial communications at a first rate with a system memory controller;

executing parallel communications with a memory array at a second rate, wherein said memory array is included on a same substrate as a high speed serial memory interface system; and

configuring said information in proper alignment for communication between serial system controller signals and parallel memory array signals.

18(Original) A high speed serial memory interface method of claim 17 further comprising:

receiving serially system memory information write signals, address signals and control signals at a relatively fast clock rate;

transmitting serially system memory information read signals at a relatively fast clock rate;

transmitting in parallel memory array information receive signals, address signals and control signals; and

receiving in parallel memory array information transmit signals at a relatively slow clock rate.

19(Original) A high speed serial memory interface method of claim 17 wherein data and address bits are provided synchronously upon a clock signal edge.

20(Original) A high speed serial memory interface method of claim 17 wherein signals on a transmit channel are phase aligned, encoded and serialized, and signals on a receive channel are deserialized, framed, decoded and buffered.

21(Previously Presented) A high speed serial memory interface system comprising:

an information configuration core for coordinating proper alignment of information communication signals, wherein said information configuration core includes a transmit channel with:

a phase aligner for aligning signals forwarded from said memory array interface;

an encoder for encoding said signals forwarded from said memory array interface, said encoder coupled to said phase aligner; and

a serializer for serializing signals receive from said memory array interface, said serializer coupled to said encoder;

a system interface for communicating with a system controller at a first communication rate, said system interface coupled to said information configuration core; and

a memory array interface for communicating with a memory array at a second communication rate, said memory array interface coupled to said information core,

wherein said memory array is included on a same substrate as said high speed serial memory interface system.

22(Previously Presented) A high speed serial memory interface system comprising:

an information configuration core for coordinating proper alignment of information communication signals, wherein said information configuration core includes a receive channel with:

a deserializer for deserializing information received from said system interface;

a framer for framing information received from said system interface to its byte boundary, said framer coupled to said deserializer;

a decoder for decoding information received from said system interface, said decoder coupled to said framer; and

an elasticity buffer for buffering information received from said system interface, said elasticity buffer coupled to said decoder;

a system interface for communicating with a system controller at a first communication rate, said system interface coupled to said information configuration core; and

a memory array interface for communicating with a memory array at a second communication rate, said memory array interface coupled to said information core, wherein said memory array is included on a same substrate as said high speed serial memory interface system.